EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5	(("6526340") or ("6810042") or ("5745048") or ("6105080") or ("6356823")).PN.	USPAT	OR	OFF	2007/01/30 10:15
L2	2809	((703/28,21) or (701/29,35,102)).CCLS.	USPAT	OR	OFF	2007/01/30 10:50
L3	81	2 and FPGA	USPAT	OR	OFF	2007/01/30 10:16
L4	3052	((703/28,21,24) or (701/29,35,102)).CCLS.	USPAT	OR	OFF	2007/01/30 10:47
L5	15	4 and FPGA and PCI and BUS	USPAT	OR	OFF	2007/01/30 10:50
L6	2244	(701/29,35,102).CCLS.	USPAT	OR	OFF	2007/01/30 10:50
L7	20	6 and FPGA	USPAT	OR	OFF	2007/01/30 10:54
L8	24	(ignition adj switch) and ((free adj run) with timer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/30 10:56

Published before January 2003
Terms used **peripheral pci fpga logic development**

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Relevance scale

1 Development of PPRAM-link interface (PLIF) IP core for high-speed inter-SoC communication

Takanori Okuma, Koji Hashimoto, Kazuaki Murakami

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation ASP-DAC '01**

Publisher: ACM Press

Full text available: pdf(105.34 KB) Additional Information: full citation, abstract, references, index terms

We are proposing "PPRAM-Link": a new high-speed communication standard for merged-DRAM/logic SoC architecture. PPRAM-Link standard is composed of physical/logical layers and an API for the upper software layer, which are standardized by PPRAM Consortium. We developed a PPRAM-Link Interface IP family, or "PLIF Core" that realizes logical protocols necessary for subaction-level communications, and it can be applied to various applications. In addition, we designed an FPGA-based PCI-to-PPRAM-L ...

2 Virtual Java/FPGA interface for networked reconfiguration

Yajun Ha, Geert Vanmeerbeeck, Patrick Schaumont, Serge Vernalde, Marc Engels, Rudy Lauwereins, Hugo De Man

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation ASP-DAC '01**

Publisher: ACM Press

Full text available: pdf(242.47 KB) Additional Information: full citation, abstract, references, citings, index terms

A virtual interface between Java and FPGA for networked reconfiguration is presented. Through the Java/FPGA interface, Java applications can exploit hardware accelerators with FPGAs for both functional flexibility and performance acceleration. At the same time, the interface is platform independent. It enables the networked application developers to design their applications with only one interface in mind when considering the interfacing issues. The virtual interface is part of our work to ...

3 A systematic approach to software peripherals for embedded systems

D. Lioupis, A. Papagiannis, D. Psihogiou

April 2001 **Proceedings of the ninth international symposium on Hardware/software codesign CODES '01**

Publisher: ACM Press

Full text available: pdf(562.90 KB) Additional Information: full citation, abstract, references, index terms

The continued growth of microprocessors' performance and the need for better CPU utilization, has led to the introduction of the software peripherals' approach: By this term we refer to software modules that can successfully emulate peripherals that, until now, were traditionally implemented in hardware. Software implementations offer great flexibility in product design and in functional upgrades, while they have high contribution in the cost/performance ratio optimization. We focus on embedd ...

Keywords: embedded processors, reconfigurable architectures, software peripherals

4 Embedded systems à la carte

Peter Ryser, Michael Baxter

August 2002 **Linux Journal**, Volume 2002 Issue 100

Publisher: Specialized Systems Consultants, Inc.

Full text available: html(20.91 KB) Additional Information: full citation, abstract, index terms

Replacing hardware on the chip while dynamically loading the properLinux driver? No way!

5 The A to Z of SoCs

Reinaldo A. Bergamaschi, John Cohn

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design ICCAD '02**

Publisher: ACM Press

Full text available: pdf(209.48 KB) Additional Information: full citation, abstract, references, citings, index terms

The exploding complexity of new chips and the ever decreasing time-to-market window are forcing fundamental changes in the way systems are designed. The advent of Systems-on-Chip (SoC) based on pre-designed intellectual-property (IP) cores has become an absolute necessity for embedded systems companies to remain competitive. Designing an SoC, however, is extremely complex, as it encompasses a range of difficult problems in hardware and software design. This paper explains a wide range of SoC iss ...

6 Re-configurable computing in wireless

Bill Salefski, Levent Caglar

June 2001 **Proceedings of the 38th conference on Design automation DAC '01**

Publisher: ACM Press

Full text available: pdf(240.76 KB) Additional Information: full citation, abstract, references, citings, index terms

Wireless communications requires a new approach to implement the algorithms for new standards. The computational demands of these standards are outstripping the ability of traditional signal processors, and standards are changing too quickly for traditional hardware implementation. In this paper we outline how reconfigurable processing can meet the needs for wireless base station design while providing the programmability to allow not just field upgrades as standards evolve, but also to a ...

7 How Do You Design a 10M Gate ASIC?: Going mobile: the next horizon for multi-million gate designs in the semi-conductor industry

Christian Berthet

June 2002 **Proceedings of the 39th conference on Design automation DAC '02**

Publisher: ACM Press

Full text available: pdf(145.55 KB) Additional Information: full citation, abstract, references, citings, index terms

The complexity of a System-on-Chip design is not only in the million transistors packed in a square millimeter. The major challenge for technical success of a SoC is to make sure that millions lines of software fit in with millions gates. In this paper, the problematic of multi-million gate design is illustrated from the viewpoint of a practical development of a complex digital system done at STMicroelectronics for a GSM/GPRS cellular application.

Keywords: HW/SW co-design, SoC design

8 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Publisher: ACM Press

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

9 An Object-Oriented Communication Library for Hardware-Software CoDesign

Frank Vahid, Linus Tauro

March 1997 **Proceedings of the 5th International Workshop on Hardware/Software Co-Design CODES '97**

Publisher: IEEE Computer Society

Full text available: pdf(858.92 KB) Publisher Site Additional Information: full citation, abstract, citings

Implementing communication between hardware and software components can be a time-consuming task. Numerous communication protocols are available, differing greatly in their implementation details. Designers must spend much time focusing on those details. Even when libraries are available to encapsulate communication into C or VHDL routines, these routines are not consistent across protocols, making it difficult to switch to other protocols. In this paper, we propose an object-oriented communicat ...

Keywords: Communication, Libraries, Object-Oriented, C, VHDL, Codesign

10 Windows NT software design and implementation for a wireless LAN base station

Marko Hännikäinen, Timo Vanhatupa, Jussi Lemiläinen, Timo Hämäläinen, Jouka Saarinen

August 1999 **Proceedings of the 2nd ACM international workshop on Wireless mobile multimedia WOWMOM '99**

Publisher: ACM Press

Full text available: pdf(1.20 MB) Additional Information: full citation, references, index terms

Keywords: Windows NT, demostrator platform, wireless LAN

11 Networked surfaces: a new concept in mobile networking

James Scott, Frank Hoffmann, Mike Addlesee, Glenford Mapp, Andy Hopper

October 2002 **Mobile Networks and Applications**, Volume 7 Issue 5

Publisher: Kluwer Academic Publishers

Networked Surfaces are surfaces which provide networking to specially augmented objects when these objects are physically placed on top of the surface. When an object (e.g., a notebook computer) connects, a handshaking protocol assigns functions such as data or power transmission to the various conducting paths that are established. This paper describes the position occupied by this concept in the world of networking, presents an overview of the technology used in its realisation, describes the ...

Keywords: mobile networking, sentient computing, ubiquitous computing

Results 1 - 11 of 11

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	9	(PCI with core) and Xilinx.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/30 14:23
L2	0	(PCI with core) and busmaster and fpga	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/30 14:24
L3	208	(PCI with core) and fpga	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/30 14:24
L4	199	3 not 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/30 14:24
L5	10	("3473160" | "4060713" | "4174514" | "4509187" | "5146608" | "5635851" | "5887138" | "6226738" | "6504786").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/01/30 14:38

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» Key

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **Design of low cost FPGA based PCI Bus Sniffer**
   Chee Wei Liang; Zain Ali, N.B.; Seth Nair, R.;
   Field-Programmable Technology (FPT), 2003. Proceedings. 2003 IEEE Interna Conference on
   15-17 Dec. 2003 Page(s):420 - 423
   Digital Object Identifier 10.1109/FPT.2003.1275792
   AbstractPlus | Full Text: PDF(326 KB) IEEE CNF
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2. **A PCI-compatible FPGA-coprocessor for 2D/3D image processing**
   Knittel, G.;
   FPGAs for Custom Computing Machines, 1996. Proceedings. IEEE Symposiu
   17-19 April 1996 Page(s):136 - 145
   Digital Object Identifier 10.1109/FPGA.1996.564782
   AbstractPlus | Full Text: PDF(900 KB) IEEE CNF
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3. **A plug and play approach to data acquisition**
   Toledo, J.; Muller, H.; Buytaert, J.; Bal, F.; David, A.; Guirao, A.; Mora, F.J.;
   Nuclear Science, IEEE Transactions on
   Volume 49, Issue 3, Part 2, June 2002 Page(s):1190 - 1194
   Digital Object Identifier 10.1109/TNS.2002.1039635
   AbstractPlus | References | Full Text: PDF(219 KB) IEEE JNL
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4. **PCI Express multi-lane de-skew logic design using embedded SERDES F**
   Won-ok Kwon; Hyuk-je Kwon; Kyoung Park;
   Solid-State and Integrated Circuits Technology, 2004. Proceedings. 7th Interna Conference on
   Volume 3, 18-21 Oct. 2004 Page(s):2035 - 2038 vol.3
   Digital Object Identifier 10.1109/ICSICT.2004.1435242
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5. **A system for fault detection and reconfiguration of hardware based activ**
   Bartzoudis, N.G.; Fragkiadakis, A.G.; Parish, D.J.; Nunez, J.L.;
   On-Line Testing Symposium, 2004. IOLTS 2004. Proceedings. 10th IEEE Inter
   12-14 July 2004 Page(s):207 - 213